What is claimed is:

1. A flash memory device comprising:

a memory array; and

a check register to store an access code, wherein the check register allows write operations to the memory array in response to the access code.

2. The flash memory device of claim 1 wherein the check register toggles a write enable signal in response to an externally provided access code.

3. The flash memory device of claim 1 wherein the check register is volatile so the access code is erased when power is removed from the check register.

4. The flash memory device of claim 1 wherein the access code is randomly generated by a program executed by a processor.

5. The flash memory device of claim 4 wherein the program is generally executed immediately after power is applied to the processor.

6. A flash memory system comprising:

a flash memory array having a BIOS program stored therein, wherein the BIOS program contains a program to generate a random access code when executed by a processor; and

a check register to store the random access code, wherein the check register enables write operations to the flash memory array based upon an externally provided access code.

7. The flash memory system of claim 6 wherein the BIOS program directs the processor to write the random access code to the check register to enable write operations in response to an external write request.

8. The flash memory system of claim 6 wherein the program to generate the access code is located in a portion of the flash memory array that is protected from being written over.

9. The flash memory system of claim 6 wherein the check register further comprises:

a compare register to store codes;

an access code register to store the random access code; and

a register control circuit to compare a code stored in the compare register to the random access code, wherein the register control circuit enables write operations when a code written to the compare register matches the random access code.

10. The flash memory system of claim 9 wherein the first write of a code to the compare register after boot up is stored in the access code register.

11. A flash memory system comprising:

a processor to process data;

a memory array storing a BIOS program to instruct the processor to generate an access code; and

a check register to store the access code generated by the processor, wherein the check register enables write operations to the memory array in response to writes of the access code.

12. The flash memory system of claim 11 wherein the BIOS program instructs the processor to generate the access code at each system power up.

13. The flash memory system of claim 11 wherein the BIOS program controls writes of the access code to the check register.

14. The flash memory system of claim 13 wherein a utility program requests the BIOS to write the access code to the check register.

15. The flash memory system of claim 13 wherein an external program requests the BIOS to write the access code to the check register.

16. A flash memory system comprising:

a processor to process data;

a memory array storing a BIOS program, the BIOS program containing a program to instruct the processor to generate an access code at power up;

control circuitry to control write operations to the memory array in response to a write enable signal; and

a check register to store the access code generated by the processor, wherein the check register toggles the write enable signal in response to writes of the access code.

17. The flash memory system of claim 16 wherein the first write to the check register of the access code sets the access code in the check register.

18. The flash memory system of claim 16 wherein a write operation request to the memory array must contain an authorization code that is recognized by the BIOS program.

19. The flash memory system of claim 16 wherein the write enable signal is toggled between an inactive HIGH signal and an active LOW signal.

20. The flash memory system of claim 19 further comprising:

a logic circuit to supply an inactive HIGH write enable signal to the control circuitry upon completion of a write operation to the memory array.

21. The flash memory system of claim 16 wherein the write enable signal is toggled between an inactive LOW signal and an active HIGH signal.

22. The flash memory system of claim 20 further comprising:

a logic circuit to supply an inactive LOW write enable signal to the control circuitry upon completion of a write operation to the memory array.

23. A flash memory system comprising:

a memory array having a BIOS program;

a processor to execute the BIOS program;

control circuitry to control write operations to the memory array in response to a write enable signal; and

a check register to store a random access code generated by the BIOS program, wherein the check register gates the write enable signal to the control circuitry in response to the random access code.

24. The flash memory device of claim 23 wherein the random access code is stored in volatile memory so the random access code is erased when power is removed from the check register.

25. The flash memory system of claim 23 wherein the memory array and the check register are embedded in a single flash memory.

26. The flash memory system of claim 23 wherein the check register is not located inside the flash memory that contains the flash memory array.

27. The flash memory system of claim 26 further comprising:

a serial bus to couple the check register to the processor.

28. A flash memory system comprising:

a memory array having a BIOS program stored therein;

control circuitry to control write operations to the memory array;

a processor to execute the BIOS program; and

a program logic device to store a random access code generated by the processor from instructions contained in the BIOS program, wherein the program logic device gates a write enable signal to the control circuitry in response to the random access code.

29. The flash memory system of claim 28 wherein the random access code is specific to each boot cycle.

30. The flash memory system of 28 wherein the program logic device further comprises:

a check register to send an active LOW write enable signal to the control circuitry in response to the random access code being written to the check register, wherein the control circuitry allows write operations to the memory array; and

a logic circuit to selectively send an inactive HIGH signal to the control circuitry after completion of the write operation to the flash memory array to disable write operations to the memory array.

31. The flash memory system of 30 wherein an output of the processor supplying write enable signals is coupled to a first input of the logic circuit and an output of the check register is coupled to a second input of the logic circuit, further wherein an output of the logic circuit is coupled to the control circuitry.

32. The flash memory system of claim 30 wherein the logic circuit performs an AND function.

33. The flash memory system of 28 wherein the program logic device further comprises:

a check register to send an active HIGH write enable signal to the control circuitry in response to the random access code being written to the check

register, wherein the control circuitry allows write operations to the memory array; and

a logic circuit to selectively send an inactive LOW signal to the control circuitry after completion of the write operation to the flash memory array to disable write operations to the memory array.

34. The flash memory system of 33 wherein an output of the processor supplying write enable signals is coupled to a first input of the logic circuit and an output of the check register is coupled to a second input of the logic circuit, further wherein an output of the logic circuit is coupled to the control circuitry.

35. The flash memory system of claim 33 wherein the logic circuit performs an AND function.

36. A processor system comprising:

a non-volatile memory device;

a code register coupled to the non-volatile memory device; and

a processor coupled to provide a request code to the code register, wherein the code register controls a write enable signal of the non-volatile memory device.

37. The processor system of claim 36 wherein the code register is volatile.

38. The processor system of claim 36 wherein the processor generates an enable code and programs the enable code in the code register.

39. The processor system of claim 38 wherein the code register compares the request code to the enable code to control the write enable signal.

40. The processor system of claim 38 wherein the processor generates the enable code while executing a basic input/output program (BIOS).

41. The processor system of claim 40 wherein the BIOS is stored in the non-volatile memory.

42. A method of operating a flash memory comprising:

generating a random access code at power up;

writing the access code to a check register; and

toggling write enable signals in response to writes of the access code to the check register.

43. The method of claim 42 wherein a BIOS program stored in the flash memory instructs a processor to generate the access code.

44. The method of claim 42 wherein the BIOS program controls the writes of the access code to the check register.

45. A method of operating a flash memory system comprising:

powering up a flash memory;

executing a BIOS program;

generating a random access code in response to the executed BIOS program;

storing the random access code in a check register; and

toggling write enable signals of the flash memory in response to writes of the random access code to the check register.

46. The method of claim 45 further comprising:

monitoring a write request to the flash memory for an authorization code; and

writing the access code to the check register if the write request has the authorization code.

47. The method of claim 46 wherein a BIOS program controls writes of the random access code to the check register.

48. The method of claim 46 wherein the BIOS program authenticates the authorization code.

49. A method of operating a flash memory system comprising:

generating a random access code at power up;

storing the random access code in a check register that controls a write enable signal to a flash memory;

executing a utility program containing instructions to write to the flash memory;

verifying the authenticity of the utility program;

toggling the check register to assert the write enable signal;

writing to the flash memory array; and

toggling the check register to disable the write enable signal.

50. The method of claim 49 further comprising:

deleting the random access code when power is removed from the flash memory system.

51. The method of claim 49 wherein a BIOS controls the toggling of the write enable signals by writing the random access code to the check register.

52. The method of claim 49 wherein the BIOS authenticates the utility program.

53. A method of operating a flash memory system comprising:

executing a utility program containing instructions to write to a flash memory array;

verifying the authenticity of the utility program with a BIOS program;

asserting a write enable signal if the utility program is authenticated; and

writing to the flash memory array.

54. The method of claim 53 wherein the BIOS program controls the write enable signals.

55. The method of claim 53 wherein the BIOS program writes an access code to a check register to toggle the write enable signals.

56. A method of operating a memory system comprising:

generating an enable code;

issuing a write request from a processor, the write request comprises a request code; and

comparing the request code to the enable code and providing a write enable signal to a memory device in response to the comparison.

57. The method of claim 56 wherein the enable code is generated by the processor.

58. The method of claim 57 wherein the processor generates the enable code while executing a BIOS program during an initialization operation of the processor.

59. The method of claim 58 wherein the BIOS program is stored in a memory.